AMENDMENTS TO THE CLAIMS

1. (original) A memory read circuit, comprising:

a plurality of memory cells, each being configured to store data as an energy-absorbing state;

a conductor line electrically coupled to each of said plurality of memory cells; and

a fast fourier transform analysis circuit electrically coupled to said conductor line, wherein said plurality of memory cells, said conductor line and said fast fourier transform analysis circuit are configured to read data stored in each of said plurality of memory cells in response to a read signal applied to said conductor line.

2. (original) The read memory circuit of claim 1, wherein said memory cells are zero field splitting resonance memory cells.

3. (original) The read memory circuit of claim 1, wherein said memory cells are PCRAM cells.

4. (original) The read memory circuit of claim 1, wherein said memory cells are MRAM cells.

5. (original) The read memory circuit of claim 1, wherein said memory cells are polymer memory cells.

6. (original) The read memory circuit of claim 1, wherein said memory cells are chalcogenide memory cells.

7. (original) The read memory circuit of claim 1, wherein said memory cells are differential negative resistance memory cells.

8. (original) The read memory circuit of claim 1, wherein said memory cells comprise a host material incorporating metal ions, said host material and metal ions being configured to absorb a detectable amount of energy corresponding to a separation in energy of the electron spin levels of said metal ions at zero field.

9. (original) The read memory circuit of claim 8, wherein said host material and said metal ions are configured to absorb about 0.03 cm^{-1} to about 3.3 cm^{-1} when programmed to an energy absorbing state.

10. (original) The read memory circuit of claim 8, wherein said host material and said metal ions are configured to absorb about 0.33 cm^{-1} at a frequency of about 9.68 GHz when a respective memory cell is programmed to said energy-absorbing state.

11. (original) The read memory circuit of claim 1, wherein the configuration of said plurality of memory cells, said conductor line and said fast fourier transform analysis circuit can provide a signature pulse out potential shape during a read operation, said signature pulse out potential shape representing the programmed state of each of said plurality of memory cells.

12. (original) The read memory circuit of claim 11, wherein said signature pulse out potential shape is defined by the programmed state of said plurality of memory cells and the location of each along said conductor line.

13. (original) The read memory circuit of claim 1, wherein said conductor line is a column line.

14. (original) A memory read circuit, comprising:

a plurality of memory cells, each comprising a first electrode and a second electrode electrically coupled to a host material incorporating metal ions, said metal ions exhibiting zero field splitting resonance, said host material and metal ions being configured to store data as an energy-absorbing state and a non-energy-absorbing state;

a conductor line electrically coupled to each of said plurality of memory cells; and

a fast fourier transform analysis circuit electrically coupled to said conductor line, wherein said plurality of memory cells, said conductor line and said fast fourier transform analysis circuit are configured to read data stored in each of said plurality of memory cells in response to a read signal applied to said conductor line.

15. (original) The read memory circuit of claim 14, wherein said host material is germanium selenide.

16. (original) The read memory circuit of claim 14, wherein said metal ions comprise Mn^{+2}.

17. (original) The read memory circuit of claim 14, wherein said host material is $Ge_{40}Se_{60}$ incorporating about 3 wt. % Mn^{+2} as said metal ions.

18. (original) The read memory circuit of claim 14, wherein said host material and said metal ions are configured to absorb a detectable amount of energy corresponding to a separation in energy of the electron spin levels of said metal ions at zero field.

19. (original) The read memory circuit of claim 14, wherein said host material and said metal ions are configured to absorb about 0.03 cm-1 to about 3.3 cm^{-1} when a respective memory cell is programmed to said energy-absorbing state.

20. (original) The read memory circuit of claim 14, wherein said plurality of memory cells are each configured to be programmed to said energy-absorbing state by a light pulse.

21. (original) The read memory circuit of claim 14, wherein said plurality of memory cells are each configured to be programmed to said energy-absorbing state by an electrical pulse.

22. (original) The read memory circuit of claim 14, wherein the configuration of said plurality of memory cells, said conductor line and said fast fourier transform analysis circuit can provide a signature pulse out potential shape during a read operation, said signature pulse out potential shape representing the programmed state of each of said plurality of memory cells.

23. (original) The read memory circuit of claim 22, wherein said signature pulse out potential shape is defined by the programmed state of said plurality of memory cells and the location of each along said conductor line.

24. (original) The read memory circuit of claim 14, wherein said conductor line is a column line.

25. (original) A processor-based device, comprising:

a processor; and

a memory read circuit, comprising:

a plurality of memory cells, each comprising a first electrode and a second electrode electrically coupled to a host material incorporating metal ions, said metal ions exhibiting zero field splitting resonance, said host material and metal ions being configured to store data as an energy-absorbing state and a non-energy-absorbing state;

a conductor line electrically coupled to each of said plurality of memory cells; and

a fast fourier transform analysis circuit electrically coupled to said conductor line, wherein said plurality of memory cells, said conductor line and said fast fourier transform analysis circuit are configured to read data stored in each of said plurality of memory cells in response to a read signal applied to said conductor line.

26. (original) The read memory circuit of claim 25, wherein said host material is $Ge_{40}Se_{60}$ incorporating about 3 wt. % Mn^{+2} as said metal ions.

27. (original) The read memory circuit of claim 25, wherein the configuration of said plurality of memory cells, said conductor line and said fast fourier transform analysis circuit can provide a signature pulse out potential shape during a read operation, said signature pulse out potential shape representing the programmed state of each of said plurality of memory cells.

28. (original) The read memory circuit of claim 27, wherein said signature pulse out potential shape is defined by the programmed state of said plurality of memory cells and the location of each along said conductor line.

29. (original) A method of simultaneously reading a plurality of memory cells, comprising:

providing a plurality of memory cells, each being programmable to an energy-absorbing state;

programming at least one of said plurality of memory cells to said energy-absorbing state; and

reading said plurality of memory cells simultaneously by sensing the absorption or transmission of a read energy pulse through each of said plurality of memory cells.

30. (original) The method of claim 29, wherein each memory cells of said plurality of memory cells is electrically connected to a conductor line, said conductor line being in electrical communication with a fast fourier transform analysis circuit.

31. (original) The method of claim 29, wherein said memory devices are zero field splitting resonance memory cells.

32. (original) The method of claim 29, wherein said memory devices are PCRAM cells.

33. (original) The method of claim 29, wherein said memory devices are MRAM cells.

34. (original) The method of claim 29, wherein said memory devices are polymer memory cells.

35. (original) The method of claim 29, wherein said memory devices are chalcogenide memory cells.

36. (original) The method of claim 29, wherein said memory devices are differential negative resistance memory cells.

37. (original) The method of claim 29, wherein said reading said plurality of memory cells comprises applying energy to each of said plurality of memory cells without changing the programming of any said memory cell.

38. (original) The method of claim 29, wherein a fast fourier transform analysis circuit is configured to interpret the read energy pulse through said plurality of memory cells as an output signature defined by the programmed state and location on a conductor line of each cell of said plurality of memory cells.

39. (original) A method of simultaneously reading a plurality of memory cells, comprising:

providing a plurality of memory cells, each comprising a host material which incorporates metal ions exhibiting zero field splitting resonance;

interconnecting said plurality of memory cells with a conductor line in electrical communication with a fast fourier transform analysis circuit;

programming at least one cell of said plurality of memory cells to an energy-absorbing state corresponding to a separation of spin states of said metal ions at zero magnetic field; and

reading said plurality of memory cells simultaneously by sensing the absorption or transmission of a read energy pulse through said host material of said plurality of memory cells.

40. (original) The method of claim 39, wherein said host material comprises $Ge_{40}Se_{60}$ glass.

41. (original) The method of claim 39, wherein said metal ions comprise Mn^{+2}.

42. (original) The method of claim 39, wherein said reading said plurality of memory cells comprises applying energy to said host material of each memory cell of said plurality of memory cells in the microwave frequency range.

43. (original) The method of claim 39, wherein said reading said plurality of memory cells comprises applying an energy pulse to said host material of at least about 0.03 cm^{-1} at a frequency of about 9.68 GHz with a risetime of about 200 picoseconds.

44. (original) The method of claim 39, wherein said fast fourier transform analysis circuit is configured to interpret the read energy pulse through said plurality of memory cells as an output signature defined by the programmed state and location on said conductor line of each memory cell of said plurality of memory cells.

45. (original) A method of simultaneously reading a plurality of memory cells, comprising:

providing a plurality of memory cells, each comprising $Ge_{40}Se_{60}$ glass incorporating Mn^{+2} ions, each said memory cells being configured to exhibit zero field splitting resonance;

interconnecting said plurality of memory cells with a conductor line in electrical communication with a fast fourier transform analysis circuit;

programming at least one of said plurality of memory cells to an energy-absorbing state corresponding to a separation of spin states of said metal ions at zero magnetic field; and

reading said plurality of memory cells simultaneously, said reading comprising:

applying energy in the microwave frequency range to said host material of each memory cell of said plurality of memory cells without changing the programming of any said memory cell,

interpreting the absorption or transmission of said energy through said host material of said plurality of memory devices, and

utilizing said fast fourier transform analysis circuit to produce an output signature defined by the programmed state and location on said conductor line of each of said plurality of memory devices.